CLAIMS

What is claimed is:

1. In an electronic system, an interconnect comprising:

a first node;

a second node coupled to the first node, wherein the interconnect is initially configured to include the first and second nodes; and

a third node that is coupled to the interconnect after the interconnect is initially configured, wherein the first node initiates a new connect handshake with the third node by transmitting a first signal to the third node, the first node signaling that the third node has been added to the interconnect if the third node responds to the first signal by transmitting a second signal, the first node causing the interconnect to be reconfigured if the third node transmits a third signal in response to receiving the first signal

2. The interconnect of claim 1, wherein the interconnect further comprises a fourth node and the interconnect is initially configured to include the first, second, and fourth nodes, the fourth node responding to the first node signaling that the third node has been added to the interconnect by assigning an address to the third node.

3. The interconnect of claim 2, wherein the third signal is equivlent to the first signal.

4. The interconnect of claim 1, wherein the interconnect is a serial bus.

5. An electronic system comprising:
a first component;
a second component;
an interconnect coupled to the first and second components, the interconnect comprising:
a first node coupled to the first component;
a second node coupled to the first node and the second component, wherein the interconnect is initially configured to include the first and second nodes; and
a third node that is coupled to the interconnect after the interconnect is initially configured, wherein the first node initiates a new connect handshake with the third node by transmitting a first signal to the third node, the first node signaling that the third node has been added to the interconnect if the third node responds to the first signal by transmitting a second signal, the first node causing the interconnect to be reconfigured if the

third node transmits a third signal in response to receiving the first signal

6. The electronic system of claim 5, wherein the interconnect further comprises a fourth node and the interconnect is initially configured to include the first, second, and fourth nodes, the fourth node responding to the first signaling that the third node has been added to the interconnect by assigning an address to the third node.

7. The electronic system of claim 6, wherein the third signal is equivalent to the first signal.

8. The electronic system of claim 5, wherein the interconnect is a serial bus.

9. A serial bus comprising:

a plurality of nodes including a first node;

at least one point-to-point link, each point-to-point link being coupled between two nodes, wherein the serial bus is initially configured to include the plurality of nodes; and

a second node coupled to the first node that is added to the serial bus after the serial bus is initially configured, the first node transmitting a first signal to the second node in response to detecting addition of the second node to the serial bus, the first node signaling addition of the second node to the serial bus if the second node responds to the first signal by

transmitting a second signal, the first node requesting a bus reset if the second node transmits a third signal.

10. The serial bus of claim 9, wherein the third signal is equal to the first signal.

11. The serial bus of claim 10, wherein each point-to-point link includes at least one pair of differential signal lines including an A line and a B line, each differential signal line capable of being in a 1 state, a 0 state, and a Z state, the first signal having a transmitted value of AB = 1Z, and the second signal having a transmitted value of AB = 0Z.

12. The serial bus of claim 9, wherein the first node signals addition of the second node by requesting control of the serial bus and by transmitting a fourth signal to indicate the addition of the second node when the first node is granted control of the serial bus.

13. The serial bus of claim 9, wherein the plurality of nodes further comprises a bus topology manager node that responds to the addition of the second node by transmitting a fifth signal for assigning a bus address to the second node.

14. A serial bus comprising:

a plurality of nodes including a first node, wherein the serial bus is initially configured to include the plurality of nodes;

at least one point-to-point link, each point-to-point link being coupled between two nodes, wherein each point-to-point link includes at least one pair of differential signal lines including an A line and a B line, each differential signal line capable of being in a 1 state, a 0 state, and a Z state; and

a second node coupled to the first node via a second point-to-point link, the second node being added to the serial bus after the serial bus is initially configured, the first node transmitting a first signal having a value of AB = 1Z to the second node via the second point-to-point link in response to detecting addition of the second node to the serial bus, the first node signaling addition of the second node to the serial bus if the second node responds to the first signal by transmitting a second signal having a value of AB = 0Z to the first node via the second point-to-point link, the first node requesting a bus reset if the second node transmits a third signal having a value of AB = 1Z.

15. The serial bus of claim 14, wherein the first node signals addition of the second node by requesting control of the serial bus and by transmitting a NODE_ADDED_ALERT packet to indicate the addition of the second node when the first node is granted control of the serial bus.

16. The serial bus of claim 15, wherein the NODE_ADDED_ALERT packet is a PHY configuration packet having a set_root_control bit and set_gap_timer_control bit set to a logic 0 state.

17. The serial bus of claim 15, wherein the second node has its bus address set to an invalid address in response to the first node successfully signaling addition of the second node to the serial bus.

18. The serial bus of claim 15, wherein the plurality of nodes further includes a bus topology manager node, the bus topology manager node responding to the NODE_ADDED_ALERT packet by transmitting a SET_ADDRESS packet specifying a new address for a node having the invalid address.

19. The serial bus of claim 18, wherein the SET_ADDRESS packet is a PHY configuration packet having a set_root_control bit and set_gap_timer_control bit set to a logic 0 state.

20. A method for adding a new node to a previously configured serial bus comprising the steps of:

detecting addition of the new node to the serial bus by a first node that is coupled to the new node by a point-to-point link;

transmitting a YOU ARE MY CHILD signal by the first node to the new node in response to detecting the addition of the new node;

transmitting a YOU ARE MY PARENT signal by the new node to the first node in response to receiving the YOU ARE MY CHILD signal if the new node has only one connected port;

signaling addition of the new node to the serial bus by the first node if the YOU ARE MY PARENT signal is detected by the first node;

transmitting a YOU ARE MY CHILD signal by the new node to the first node if the new node has more than one connected port; and

requesting a bus reset by the first node if the new node transmits a YOU ARE MY CHILD signal.

21. The method of claim 20, wherein the step of signaling addition of the new node to the serial bus comprises the steps of:

requesting control of the serial bus by the first node;

granting control of the serial bus to the first node;

transmitting a NODE_ADDED_ALERT packet by the first node indicating addition of the new node.

22. The method of claim 21, wherein the new node is assigned an invalid bus address in response to the NODE_ADDED_ALERT packet being sent, the method further comprising the steps of:

receiving the NODE_ADDED_ALERT packet by a bus topology manager node of the serial bus;

transmitting a SET_ADDRESS packet that specifies a valid bus address;

receiving the SET_ADDRESS packet by the new node; and

setting the new node to the valid bus address in response to receiving the SET_ADDRESS packet.

23. A method for removing a first node from a previously configured serial bus comprising the steps of:

detecting by a second node that the first node has been removed;

requesting control of the serial bus by the second node;

granting control of the serial bus to the second node;

transmitting a NODE_DETACHED_ALERT packet by the second node indicating removal of the first node.

24. A node for use in an electronic system interconnect comprising:

at least one port including a first port operative to transmit and receive data when electrically connected to another node;

a first circuit coupled to the first port operative to detect when an electrical connection is made between the first port and a second node; and

a second circuit coupled to the first port operative to detect how many ports are connected to transmit and receive data after the electrical connection is made between the first port and the second node,

wherein the node is operative to initiate a new connect handshake with the second node by transmitting a first signal via the first port if the node has more than one connected port, the node being operative to wait for the second node to initiate the new connect handshake by transmitting the first signal to the node if the node has only one connected port, the node transmiting a reset request if the node and the second node contemperaneously assert the first signal.

25. The node claimed in claim 24, wherein the node transmits a reset request if the node waits a predetermined time before receiving the first signal from the second node.

26. The node claimed in claim 24, wherein the node transmits a second signal in response to receiving the first signal, the second signal completing the new connect handshake.

27. The node as claimed in claim 24, wherein the interconnect is a serial bus.

28. A method for building a topology map of an interconnect comprising the steps of:

transmitting a request packet to a first node by a topology manager node, the request packet specifying that the first node is to identify itself;

receiving the request packet by the first node;

transmitting a first identity packet by the first node in response to the request, the first identity packet specifying a bus address of the first node;

receiving the first identity packet by the topology manager node; and

identifying a location of the first node in the interconnect by the topology manager.

29. The method of claim 28, further comprising the steps of:

transmitting a second identity packet by a parent node of the first node in response to the first node transmitting the first identity packet after the first node transmits the first identity packet, the second identity packet specifying a bus address of the parent node; and

receiving the second identity packet by the topology manager node after the first identity packet is received, wherein the topology manager identifies locations in the interconnect for both the first node and the parent node.

30. The method of claim 28, wherein the interconnect is a serial bus and the request packet is a SEND_SELF_ID packet.

31. The method of claim 30, wherein the first identity packets is a SELF_ID packet.

32. A serial bus comprising:

a plurality of nodes including a bus topology manager node, a target node, and a parent node of the target node; and

at least one point-to-point link, each point-to-point link being coupled between two nodes, wherein the bus topology manager node transmits a request packet to target node, the target node responding to the request packet by transmitting a first identity packet of the target node to the bus topology manager, the parent node subsequently transmitting a second identity packet of a parent node in response to the target node sending the first identity packet, the bus topology manager node sequentially receiving the first and second identity packets and identifying locations of the target and parent nodes in the serial bus.

33. A node for use in an electronic system interconnect, comprising:

a first port operative to transmit and receive data via the serial bus;

a first circuit coupled to the first port operative to detect receipt by the first port of a first identity request packet addressed to the node; and

a second circuit coupled to the first circuit and the first port, the second circuit operative to transmit a first identity packet via the first port if a first identity request packet is received, the first identity packet specifying a bus address of the node.

34. The node of claim 34, further comprising:

a second port operative to transmit and receive data via the serial bus, the second port being coupled to a second node such that the node is a parent of the second node, wherein the second circuit is further operative to transmit the first identity packet if the second node transmits a second identity packet specifying a bus address of the second node.